REMARKS

Claims 1-18, 20-28 are pending. Claims 1-27 are rejected. Claim 19 has been canceled without prejudice. Upon review, the Applicants discovered that two different Claims 24 were mistakenly presented. The second Claim 24 has been renumbered Claim 28. Claims 1, 5, 10, 13-14, 20-23, 25, and 28 have been amended. No new matter has been added.

35 U.S.C. 102(b) Rejections

Claims 1-3, 5-6, 8, 10-13, 15, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Hori, U.S. Patent No. 5,943,509.

The Examiner is respectfully directed to independent Claim 1, which has been amended to recite that an embodiment of the present invention is directed to:

> A data and communication apparatus communicatively coupled with a multi-processor shared memory multimedia chip system for providing interprocessor communication while enhancing performance of each processor integral with said multi-processor shared memory multimedia chip system, said data and communication apparatus comprising:
>
> a data memory to retrievably store data, wherein said data are readily retrievable, in a non-sequential manner, by any processor in said multi-processor shared memory multimedia chip system;
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> an instruction memory coupled with said data memory to retrievably store instructions;
>
> an incoming buffer coupled with said data memory and said instruction memory which permits transfer of data into said data and communication apparatus, said incoming buffer further adapted to provide fast access to streaming data; and
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> an outgoing buffer coupled with said data memory and said instruction memory which monitors and permits transfer of data out of said data and communication apparatus, said outgoing buffer enables said

each processor to communicate with other processors disposed within said system.

Claim 10 recites similar limitations. Claims 2-3, 5-6, and 8 are dependent upon Claim 1, and recite further features of the claimed invention. Claims 11-13, 15, and 17 are dependent upon Claim 10, and recite further features of the claimed invention.

The rejection suggests that Hori discloses every element of the embodiment of the present invention disclosed in Claim 1. The Applicants have reviewed the cited portions of Hori, and respectfully disagree. The Applicants assert that Hori does not disclose a data memory to retrievably store data, wherein said data are readily retrievable, in a non-sequential manner, by any processor in said multi-processor shared memory multimedia chip system as claimed. The portion of Hori cited by the rejection discloses the use of a First-In First-Out (FIFO) component coupled with a selector component; when the selector is set one way, only the first processor would be able to read from the FIFO, and when set the other, only the second processor would be able to read from the FIFO, as described in col. 4, ln. 18-28. This is distinctly different from the embodiment of the present invention disclosed in Claims 1 and 10, which allow for access to the data stored in the data memory by any processor within the system. Moreover, one having ordinary skill in the art would know that a FIFO is limited to queue-like access, where information may only be read out in the same order it was entered. This behavior is distinctly different from that of data memory that allows for non-sequential access, which allows for data to be read in any order. Therefore, Hori does not anticipate or render obvious the embodiments of the invention described in Claims 1 and 10.

Further, the Applicants assert that Hori does not disclose an instruction memory coupled with said data memory to retrievably store instructions, as claimed. The portion of Hori cited by the rejection discloses the use of request and notification circuits, as described in col. 4, ln. 1-18. The request circuits, in the device described in Hori, allow one processor to request another to read from a FIFO. The notification circuits seem to fulfill an error-correction role, notifying the processors if data read from a FIFO is irregular. Neither of these types of circuits allows for instruction storage and retrieval, as disclosed and claimed by the present invention. Rather, the Applicants understand these components to be limited to requests for information from one processor to another. Therefore, Hori does not anticipate or render obvious the embodiments of the invention described in Claims 1 and 10.

Moreover, the Applicants assert that Hori does not disclose an incoming buffer coupled with said data memory and said instruction memory which permits transfer of data into said data and communication apparatus, said incoming buffer further adapted to provide fast access to streaming data, as claimed. The portion of Hori cited by the rejection discusses the operation of a FIFO, positioned in the system so as to allow data to pass from one processor in the described system to another. Hori does not, however, disclose an incoming buffer which permits transfer of data *into the data and communication apparatus*, as claimed. Therefore, Hori does not anticipate or render obvious the embodiments of the invention described in Claims 1 and 10.

Finally, the Applicants assert that Hori does not disclose an outgoing buffer coupled with said data memory and instruction memory which monitors and permits transfer of data out of said data and communication apparatus, said outgoing buffer enabling each said processor to communicate with other processors disposed within said system, as claimed. The portion of Hori cited by the rejection discusses the operation of "output circuits", col. 4, ln. 19-34. The Applicants understand these output circuits to function as logical gates, either allowing or preventing information flow out of a FIFO in a particular direction, as dictated by the selector switch; such operation is mentioned in col. 5, ln. 36-45 and col. 6, ln. 36-41. Hori does not teach an outgoing buffer which monitors and permits transfer of data out of a data and communication apparatus, as claimed; the output circuits described in Hori serve no monitoring function. Therefore, Hori does not anticipate or render obvious the embodiments of the invention described in Claims 1 and 10.

Therefore, the Applicants respectfully submit that the claimed embodiments of the invention as set forth in Claims 1 and 10 are in condition for allowance. Accordingly, the Applicants also respectfully submit that Claims 2-3, 5-6, and 8, dependent on Claim 1, and Claims 11-13, 15, and 17, dependent upon Claim 10, overcome the basis for rejection under 35 U.S.C. 103(a), as they are dependent on allowable base claims.

Claims 19-21, 23, 25, and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Hori, U.S. Patent No. 5,943,509. Claim 19 has been canceled without prejudice.

The Examiner is respectfully directed to independent Claim 20, which, as amended, recites that an embodiment of the present invention is directed to:

> In a multi-processor shared memory multimedia chip system having a memory space (bus) and an I/O space (bus), a method to provide interprocessor communication while enhancing processor performance, said method comprising the steps of:
>
> providing an data and communication apparatus adapted to be communicatively coupled to said multi-processor shared memory multimedia chip system, wherein access to said data and communication apparatus is via said I/O space, said data and communication apparatus further adapted to enable said interprocessor communication and said enhanced processor performance; and
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> providing a data memory to retrievably store data, wherein said data are readily retrievable, in a non-sequential manner, by any processor in said multi-processor shared memory multimedia chip system.

Claims 21, 23, 25, and 27 are dependent upon Claim 20, and recite further features of the claimed invention.

The rejection suggests that Hori discloses every step of the embodiment of the present invention disclosed in Claim 20. The Applicants have reviewed the cited portions of Hori, and respectfully disagree. The Applicants assert that Hori does not disclose a data memory to retrievably store data, wherein said data are readily retrievable, in a non-sequential manner, by any processor in said multi-processor shared memory multimedia chip system as claimed. The portion of Hori cited by the rejection discloses the use of a First-In First-Out (FIFO) component coupled with a selector component; when the selector is set one way, only the first processor would be able to read from the FIFO, and when set the other, only the second processor would be able to read from the FIFO, as described in col. 4, ln. 18-28. This is distinctly different from the embodiment of the

present invention disclosed in Claims 1 and 10, which allow for access to the data stored in the data memory by any processor within the system. Moreover, one having ordinary skill in the art would know that a FIFO is limited to queue-like access, where information may only be read out in the same order it was entered. This behavior is distinctly different from that of data memory that allows for non-sequential access, which allows for data to be read in any order. Therefore, Hori does not anticipate or render obvious the embodiments of the invention described in Claims 20.

Therefore, the Applicants respectfully submit that the claimed embodiment of the invention as set forth in Claim 20 is in condition for allowance. Accordingly, the Applicants also respectfully submit that Claims 21, 23, 25, and 27, dependent on Claim 20, overcome the basis for rejection under 35 U.S.C. 103(a), as they are dependent on allowable base claims.

35 U.S.C. 103(a) Rejections

Claims 5, 14, and 22 are rejected under 35 U.S.C. 103(a) as being obvious over Hori, in view of Slingwine et al., U.S. Patent No. 6,219,690 B1.

The Examiner is respectfully directed to dependent Claim 5, which recites, as amended, that an embodiment of the present invention is directed to:

> The data and communication apparatus of Claim 1 wherein said data retrievably stored in said data memory unit is real-time kernel thread context data, wherein said access to retrieve said real-time kernel thread context data is via said I/O space, such that traffic on said memory space is commensurately reduced, so as to increase speed with which thread context switching is achieved.

Claims 14 and 22 recite similar limitations.

The rejection relies upon Hori to disclose every element of the claimed embodiments of the present invention except real-time kernel thread context data wherein said access to retrieve said real-time kernel thread context data is via said I/O space, such that traffic on said memory space is commensurately reduced, so as to increase speed with which thread context switching is achieved, as claimed. The Applicants respectfully agree that Hori fails to disclose this element. Therefore, Hori does not anticipate or render obvious the embodiments of the invention described in Claims 5, 14, and 22.

The rejection suggests the combination of the disclosures of Slingwine et al. with Hori will render the embodiments of the present invention disclosed in Claims 5, 14, and 22 obvious. The Applicants have reviewed the cited references, and respectfully disagree. Slingwine et al. does not overcome the deficiencies in Hori discussed above. The cited portion of Slingwine et al discusses cache memory controllers used in place of a shared memory controller, as a means of reducing bus traffic, while maintaining data coherency, as described at col. 4, ln. 54 – col. 5, ln. 20. The Applicants assert that Slingwine et al. does not disclose access to stored real-time kernel thread context data via the I/O space, as claimed.

Moreover, the Applicants assert that Slingwine et al. does not overcome the deficiencies in Hori, as described above with regard to independent Claim 1. The cited portions of Slingwine et al. do not disclose a data memory to retrievably store data,

wherein said data are readily retrievable, in a non-sequential manner, by any processor in said multi-processor shared memory multimedia chip system; an instruction memory coupled with said data memory to retrievably store instructions; an incoming buffer coupled with said data memory and said instruction memory which permits transfer of data into said data and communication apparatus, said incoming buffer further adapted to provide fast access to streaming data; and an outgoing buffer coupled with said data memory and said instruction memory which monitors and permits transfer of data out of said data and communication apparatus, said outgoing buffer enables said each processor to communicate with other processors disposed within said system, as claimed.

Therefore, Hori, alone or in combination with Slingwine et al., fails to anticipate or render obvious the embodiments of the invention described in Claims 5, 14, and 22. Accordingly, the Applicants assert that claims 5, 14, and 22 are in condition for allowance.

Claims 7, 16, and 28 are rejected under 35 U.S.C. 103(a) as being obvious over Hori, in view of Moreno et al., U.S. Patent No. 6,711,651 B1. The Applicants note that Claim 28 was incorrectly numbered as Claim 24 in the original application, and therefore also referred to as Claim 24 in the rejection.

The Examiner is respectfully directed to dependent Claim 7, which recites, as amended, that an embodiment of the present invention is directed to:

> The data and communication apparatus of Claim 1 wherein said incoming buffer is configured as a prefetch mechanism for a particular type of data, so as to enable acceleration of the rate of said incoming buffer's decoding and parsing of header information relative to said particular data type, such that the processing time of said particular type of data is reduced.

Claims 16 and 28 recite similar limitations.

The rejection relies upon Hori to disclose every element of the claimed embodiments of the present invention except a prefetch mechanism for a particular type of data, so as to enable acceleration of the rate of said incoming buffer's decoding and parsing of header information relative to said particular data type, such that the processing time of said particular type of data is reduced, as claimed. The Applicants respectfully agree that Hori fails to disclose this element. Therefore, Hori does not anticipate or render obvious the embodiments of the invention described in Claims 7, 16, and 28.

The rejection suggests that the combination of the disclosures of Moreno et al. with those of Hori will render obvious the embodiments of the present invention disclosed in Claims 7, 16, and 28. The Applicants have reviewed the references, and respectfully disagree. The Applicants understand Moreno et al. to disclose a method for history-based movement of shared data in coherent cache memories, as stated in col. 1, ln. 10-13. Additionally, the cited portions of Moreno et al. do not purport to teach a prefetch mechanism, instead noting that some processors do include a mechanism referred to as a "prefetch buffer." The cited portions of Moreno et al. do not disclose a

prefetch mechanism for a particular type of data, *so as to enable acceleration of the rate of said incoming buffer's decoding and parsing of header information* relative to said particular data type, such that the processing time of said particular type of data is reduced, as claimed.

Moreover, the Applicants assert that Moreno et al. does not overcome the deficiencies in Hori, as described above with regard to independent Claim 1. The cited portions of Moreno et al. do not disclose a data memory to retrievably store data wherein said data are readily retrievable, in a non-sequential manner, by any processor in said multi-processor shared memory multimedia chip system; an instruction memory coupled with said data memory to retrievably store instructions; an incoming buffer coupled with said data memory and said instruction memory which permits transfer of data into said data and communication apparatus, said incoming buffer further adapted to provide fast access to streaming data; and an outgoing buffer coupled with said data memory and said instruction memory which monitors and permits transfer of data out of said data and communication apparatus, said outgoing buffer enables said each processor to communicate with other processors disposed within said system, as claimed.

Therefore, Hori, alone or in combination with Moreno et al., fails to anticipate or render obvious the embodiments of the invention described in Claims 7, 16, and 28. Accordingly, the Applicants assert that claims 7, 16, and 28 are in condition for allowance.

Claims 9, 18, and 26 are rejected under 35 U.S.C. 103(a) as being obvious over Hori, in view of Garnett et al, U.S. Patent No. 6,148,348.

The Examiner is respectfully directed to dependent Claim 9, which recites, as amended, that an embodiment of the present invention is directed to:

> The data and communication apparatus of Claim 1 wherein said outgoing buffer monitors the number of active communications within said system, such that a maximum number of active communications is not exceeded, so as to allow additional active communications to be placed within said system when said allowance will not exceed said maximum number.

Claims 18 and 26 recite similar limitations.

The rejection relies upon Hori to disclose every element of the claimed embodiments of the present invention except monitoring the number of active communications within said system, such that a maximum of active communications is not exceeded, so as to allow additional active communications to be placed within said system when said allowable will not exceed said maximum number, as claimed. The Applicants respectfully agree that Hori fails to disclose this element. Therefore, Hori does not anticipate or render obvious the embodiments of the invention described in Claims 9, 18, and 26.

The rejection suggests that the combination of the disclosures of Garnett et al. with those of Hori will render obvious the embodiments of the present invention disclosed in Claims 9, 18, and 26. The Applicants have reviewed the references, and respectfully disagree. The Applicants understand Garnett et al. to describe a mechanism

which limits the impact of an error where pending I/O operations have already been initiated by a processor or processor set, as set forth in col. 1, ln. 27-32. The cited portions of Garnett et al. do not disclose an outgoing buffer that *monitors the number of active communications within said system, such that a maximum number of active communications is not exceeded*, so as to allow additional active communications to be placed within said system when said allowance will not exceed said maximum number, as claimed. The mechanism disclosed in Garnett et al. includes a buffer for buffering write accesses initiated by processors when an error is detected; the mechanism described is not suitable for the embodiment described in Claim 9 of the present invention.

Moreover, the Applicants assert that Garnett et al. does not overcome the deficiencies in Hori, as described above with regard to independent Claim 1. The cited portions of Garnett et al. do not disclose a data memory to retrievably store data wherein said data are readily retrievable, in a non-sequential manner, by any processor in said multi-processor shared memory multimedia chip system; an instruction memory coupled with said data memory to retrievably store instructions; an incoming buffer coupled with said data memory and said instruction memory which permits transfer of data into said data and communication apparatus, said incoming buffer further adapted to provide fast access to streaming data; and an outgoing buffer coupled with said data memory and said instruction memory which monitors and permits transfer of data out of said data and communication apparatus, said outgoing buffer enables said each processor to communicate with other processors disposed within said system, as claimed.

Therefore, Hori, alone or in combination with Garnett et al., fails to anticipate or render obvious the embodiments of the invention described in Claims 9, 16, and 28. Accordingly, the Applicants assert that claims 9, 18, and 26 are in condition for allowance.

Conclusion

In light of the above-listed amendments and remarks, Applicants respectfully request allowance of the remaining Claims.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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